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OPTIMAL STRUCTURES FOR TWO DIFFERENT MULTI LEVEL INVERTER TOPOLOGIES

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ABSTRACT

In order to increase the steps in the output voltage, a new topology is recommended which benefits from a series connection of Sub-Multilevel Inverters. In the procedure described in this reference, despite all the advantages, it is not possible to produce all the steps (odd and even) in the output. In addition, for producing an output voltage with a constant number of steps, there are different configurations with a different number of components. The optimal structures for this topology are investigated for various objectives such as minimum number of switches and DC Voltage sources and minimum standing voltage on the switches for producing the maximum output voltage steps. Two new Algorithms for determining the DC Voltage source magnitudes have been proposed. Simulation results are obtained and compared to validate the proposed inverter.

Keywords *Optimal Structure, Cascaded Voltage Source, Cascaded H-Bridge Multilevel inverter, first and second algorithms and Sub-multilevel inverter.*

I. INTRODUCTION

Now a day's many industrial applications have begun to require high power. Some appliances in the industries however require medium or low power for their operation. Using a high power source for all industrial loads may prove beneficial to some motors requiring high power, while it may damage the other loads. Some medium voltage motor drives and utility applications require medium voltage. The multi level inverter has been introduced since 1975 as alternative in high power and medium voltage situations. The Multi level inverter is like an inverter and it is used for industrial applications as alternative in high power and medium voltage situations. Conventional two-level inverters are mostly used to day to generate an AC voltage from an DC voltage. The two-level inverter can only create two different output voltages for the load, $V_{dc}/2$ or $-V_{dc}/2$ (when the inverter is fed with V_{dc}). To build up an AC output voltage these two voltages are usually switched with PWM, see Figure 1.1. Though this method is effective it creates harmonic distortions in the output voltage, Electromagnetic interference and high *dv/dt* (compared to multilevel inverters). This may not always be a problem but for some applications there may be a need for low distortion in the output voltage.

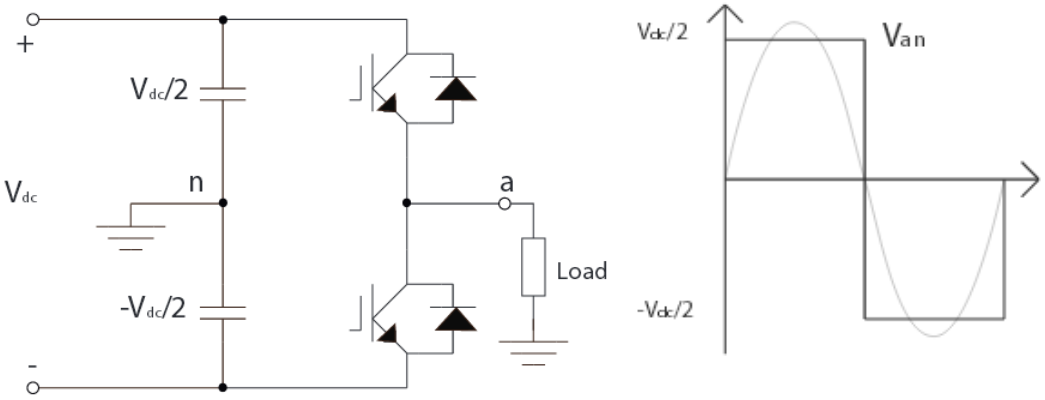

Figure 1.1 Two Level Inverters

II. MULTI LEVEL INVERTERS

The concept of Multi Level Inverters (MLI) does not depend on just two levels of voltage to create an AC signal. Instead several voltage levels are added to each other to create a smoother stepped waveform with lower *dv/dt* and lower harmonic distortions. With more voltage levels in the inverter the waveform it creates becomes smoother, but with many levels the design becomes more complicated, with more components and a more complicated controller for the inverter is needed. To better understand multilevel inverters the more conventional three-level inverter, shown in Figure 2.1, can be investigated. It is called a three-level inverter since every phase-leg can create the three

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voltages $V_{dc}/2$, *0*, $-V_{dc}/2$, as can be seen in the first part of Figure 1.2. A three-level inverter design is similar to that of a conventional two-level inverter but there are twice as many valves in each phase-leg. In between the upper and lower two valves there are diodes, called clamping diodes, connected to a neutral midpoint in between two capacitors, marked n in the figure. This capacitor build up the DC-bus, each capacitor is charged with the voltage $V_{dc}/2$. Together with another phase-leg an output line-to-line voltage with even more levels can b e obtained. To create the zero voltage the two switches closest to the midpoint are switched on and the clamping diodes hold the voltage to zero with the neutral point. Now, if more valve pairs, clamping diodes and capacitors are added the inverter can generate even more voltage levels, see Figure1.3, the result is a multilevel inverter with clamping diode topology.

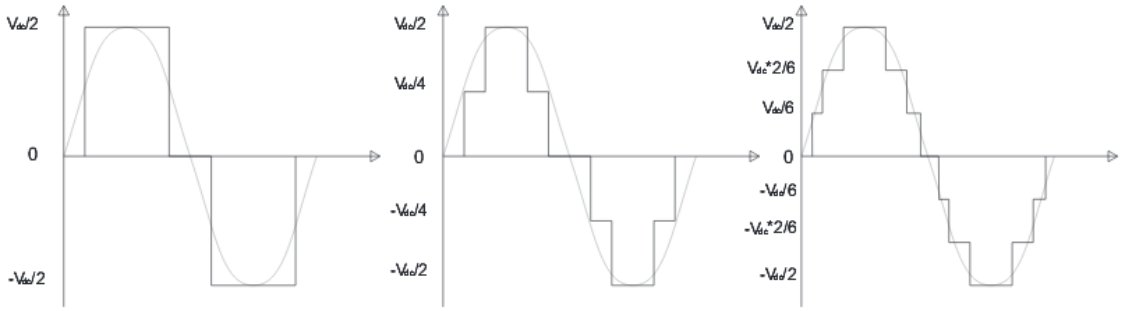
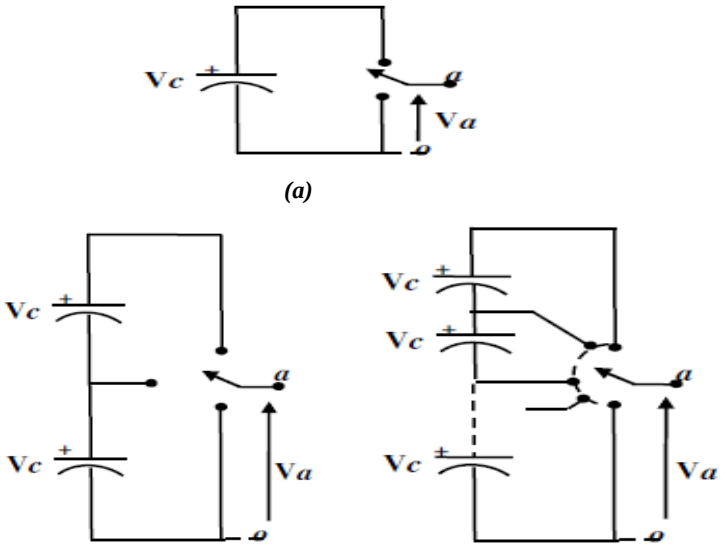


Figure 2.1 A three-level waveform, a five-level waveform and a seven-level multilevel waveform

The operation of semiconductors is shown by an ideal switch with several states. The switching pattern of switches and commutation of them allow the addition to the capacitor voltages as temporary DC voltage sources whereas the switches should withstand the voltages of capacitors. Thus Fig 2.4 shows one phase leg of multilevel inverter with different number of levels. Fig. 2.4(a) is a two-level inverter since the output voltage V_a has only two possible values while Fig. 2.4(b) is a three-level inverter since its output can have three different values. If m is the number of possible output voltage levels it is called m-level inverter shown in Fig. 2.4(c). By increasing the number of levels the output voltage waveforms will have more steps and thus have a reduced harmonic distortion. However a high number of levels will increase the complexity and introduce voltage imbalance problems.



(a) ***(b)*** ***(c)***

Figure 2.2 Single leg of multilevel inverter (a) Two level (b) Three level (c) m level

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III. PROPOSED TOPOLOGY

3.1 Topology – 1

A new topology for cascaded multilevel inverters with a high number of steps associated with a low number of switches and gate driver circuits for switches. In addition, for producing all levels (odd and even) at the output voltage, three procedures for calculating the required dc voltage sources are proposed. Finally the simulation and experimental results have proved the feasibility of the proposed multilevel inverter.

BASIC DIAGRAM FOR THE PROPOSED FIRST ALGORITHM (1:1)

Case-1(a)

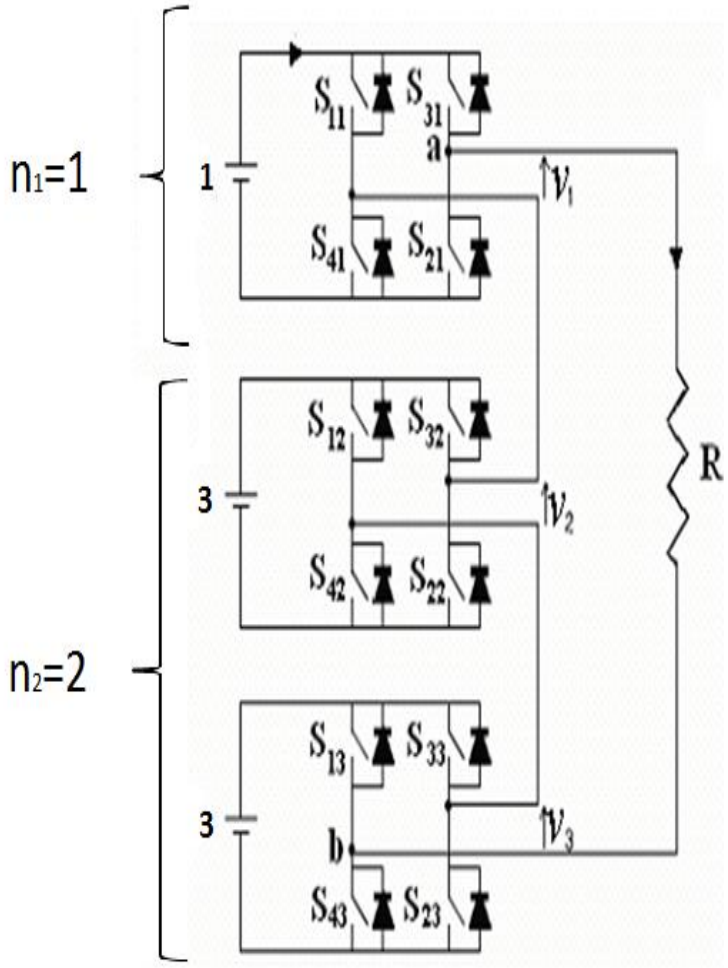

Figure 3.1 Proposed Cascaded Multilevel Inverter where $n_1 = 1$; $n_2 = 2$

Case-1(b)

The number of output voltage steps and switches are given by the following equations, respectively

$$N_{step} = \prod_{i=1}^{k}(2n_j + 1)$$

$$\boldsymbol{N_{switch} = \sum_{i=1}^{k} 4n_i}$$

The output voltage of the converter can be calculated as follows:

$$\boldsymbol{v_o(t) = \sum_{j=1}^{k} v_{o,j}}$$

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The peak value of the output voltage is calculated as follows:

$$V_{o,max} = \sum_{j=1}^{k} \sum_{i=1}^{n_j} V_{i,j}$$

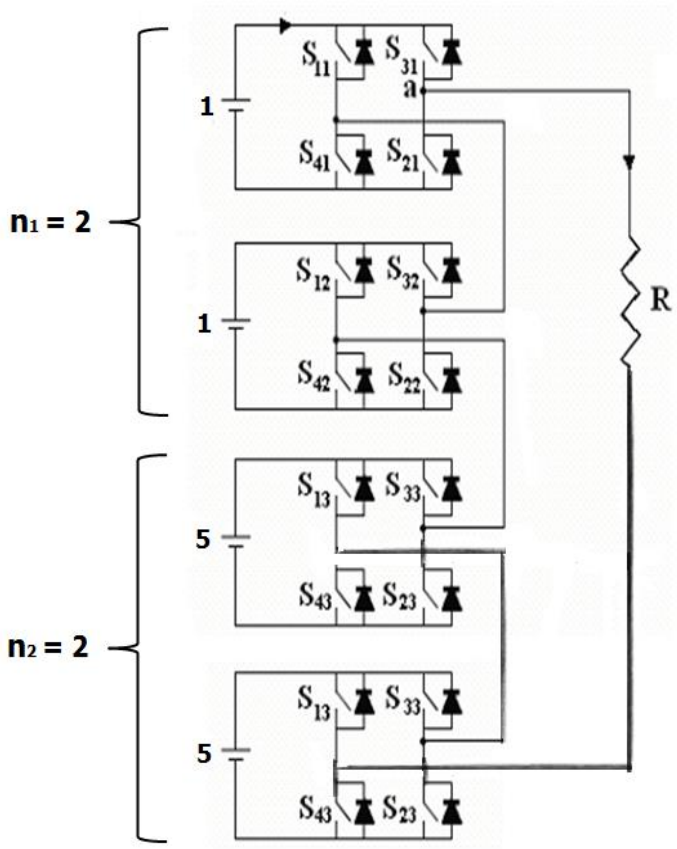

Figure 3.2 Proposed Cascaded Multilevel Inverter where $n_1 = 2;\ n_2 = 2$

FIRST PROPOSED ALGORITHM (1:1)

For a greater reduction in the variety of the values of the dc voltage sources, another new algorithm is proposed as follows

First Stage:

$V_{j,1} = V_{dc} \quad for\ j = 1, 2, 3, \dots, n_1$

$V_{1,1} = V_{dc}$

Second Stage:

$$V_{j,2} = V_{dc} + 2\sum_{i=1}^{n_1} V_{i,1} = (2n_1 + 1)V_{dc}$$

$for\ j = 1, 2, \dots, n_2$

***m*th stage:**

$$V_{j,m} = V_{dc} + 2\sum_{i=1}^{m-1} \sum_{l=1}^{n_i} V_{j,l} \qquad for\ j = 1, 2, \dots, n_m$$

This algorithm produces redundant states. In this algorithm, the number of output voltage steps is given as follows:

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$$N_{step} = \prod_{i=1}^{k}(2n_j + 1)$$

In other words, the number of redundant states in the first algorithm is less than with the second algorithm. In contrast, in the second algorithm, the variety of the values of the dc voltage sources is less than with the first algorithm.

BASIC DIAGRAM FOR THE PROPOSED SECOND ALGORITHM (1:2)

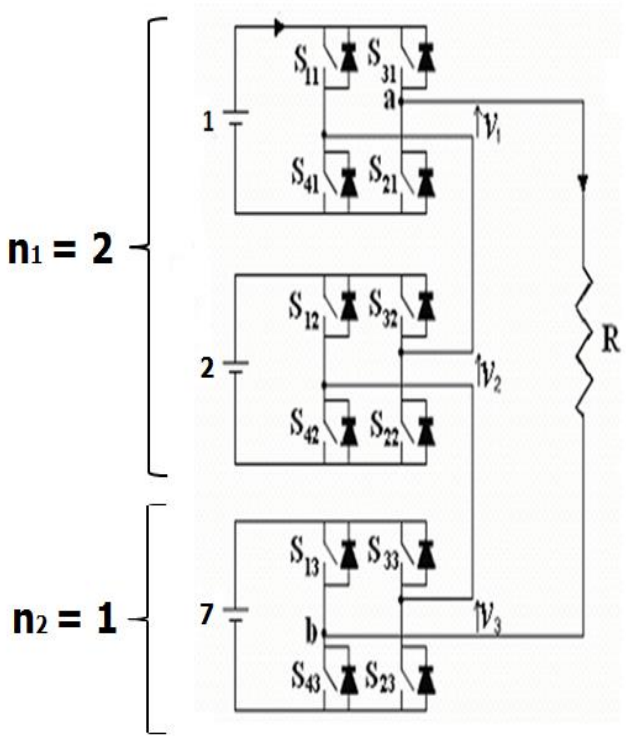

Figure 3.3 Proposed Cascaded Multilevel Inverter Second Algorithm where $n_1 = 2;\ n_2 = 1$

SECOND PROPOSED ALGORITHM (1:2)

In this algorithm it is proposed that the values for all of the dc voltage sources for generating odd and even steps can be calculated using the following relationships:

First stage:

$$V_{1,1} = V_{dc}$$

$$V_{j,1} = 2V_{dc} \quad for\ j = 2, 3, \dots, n_2$$

Second stage:

$$V_{1,2} = V_{dc} + 2\sum_{i=1}^{n1} V_{j,1} = (4n_1 - 1)V_{dc}$$

$$V_{j,2} = 2(4n_1 - 1)V_{dc} \quad for\ j = 2, 3, \dots \dots \dots, n_2$$

m-th stage:

$$V_{1,m} = V_{dc} + 2\left(\sum_{i=1}^{m-1}\sum_{j=1}^{n_i} V_{j,1}\right)$$

$$V_{j,m} = 2V_{1,m} \quad for\ j = 2, 3, \dots, n_m.$$

The disadvantage of this algorithm is that two or more switching states produce the same output voltage.

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Optimal structure for the minimum number of switches with a constant number of dc voltage sources

$$\boldsymbol{N_{switch} = [2(n_1 + 1)] + [2(n_2 + 1)] + \cdots + [2(n_k + 1)]}$$

It is obvious that by this topology the minimum number of voltage steps can be produced.

Optimal structure for the minimum number of switches with constant number of voltage steps

$$\boldsymbol{N_{switch} = \frac{4(n)}{\ln[2n + 1]} \ln N_{step.}}$$

Since N_{step} is constant, N_{switch} will be minimized when $4n = \ln[2n + 1]$ tends to the minimum. It is clear that the minimum number of switches is obtained for $n = 2$. Therefore, a structure consisting of a series of extended basic units with two dc voltage sources can provide the maximum step voltages for V_o. shows the corresponding structure. It is necessary to point out that the number of components and the number of series units is integers.

Optimal structure for the Minimum number of DC Voltage Source with a constant number of voltage steps

$$\boldsymbol{N_{capacitor} = \frac{n}{\ln[n(n + 1) + 1]} \ln N_{step.}}$$

Since N_{step} is constant, $N_{capacitor}$ will be minimized when $n = \ln[n(n + 1) + 1]$ tends to minimum..

3.2 Topology – 2

PROPOSED TOPOLOGY OF FIVE-LEVEL TRANSISTOR CLAMPED H-BRIDGE

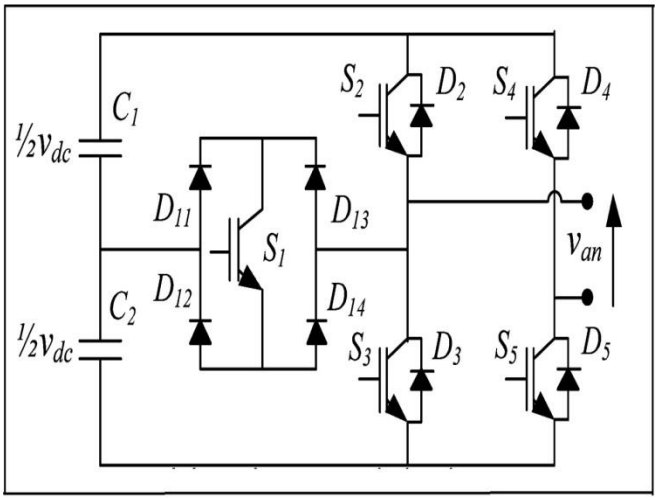

Figure 3.4 Proposed 5 level Transistor Clamped H-Bridge Topology

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BASIC DIAGRAM FOR THE PROPOSED FIRST ALGORITHM (1:1)
CASE-1:

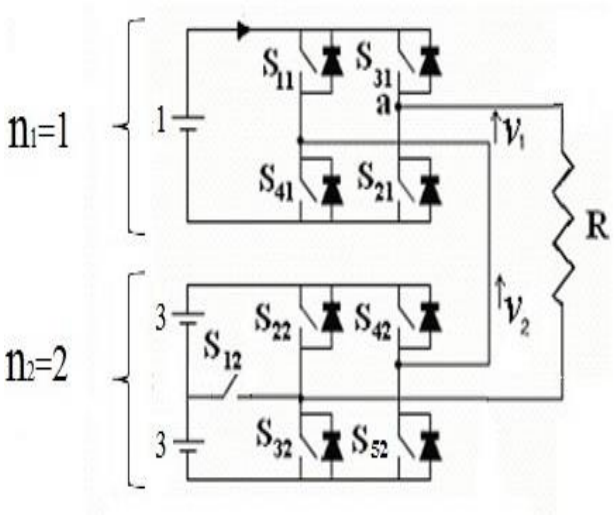

Figure 3.5: Proposed 5 level Transistor Clamped Multilevel Inverter First Algorithm where $n_1 = 1$; $n_2 = 2$

IV. SIMULATION RESULTS AND DISCUSSION

4.1 Topology – 1
SIMULATION RESULTS FOR THE FIRST PROPOSED SYSTEM:

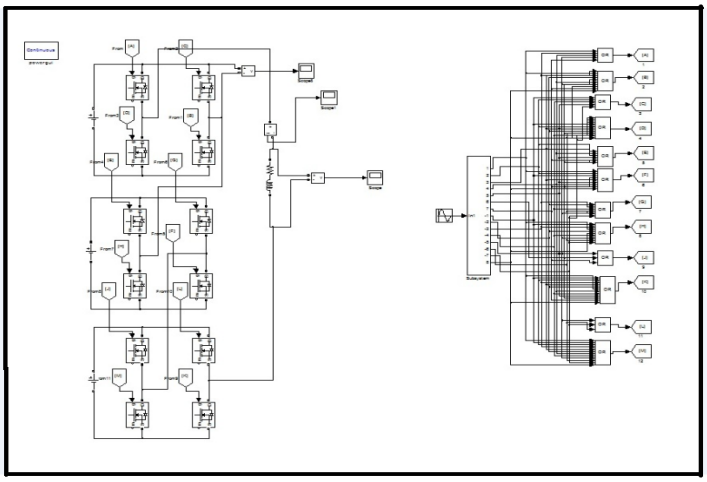

Figure 4.1 Simulink model of Optimal Structure (First Algorithm) for Cascaded Multilevel DC link Inverter

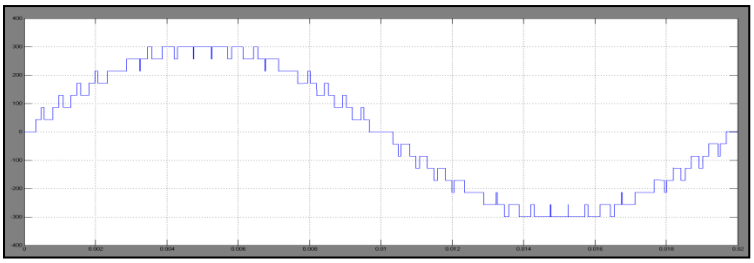

Figure 4.2: Output voltage Waveform for the First proposed system

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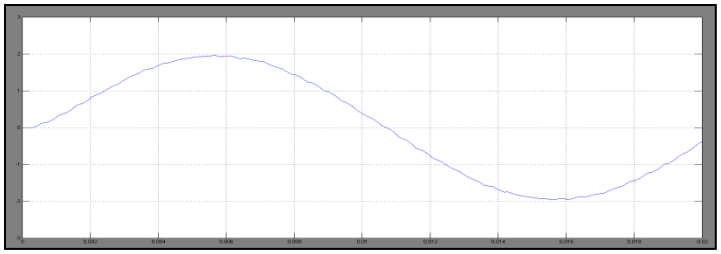

Figure 4.3: Output current Waveform for the First proposed system

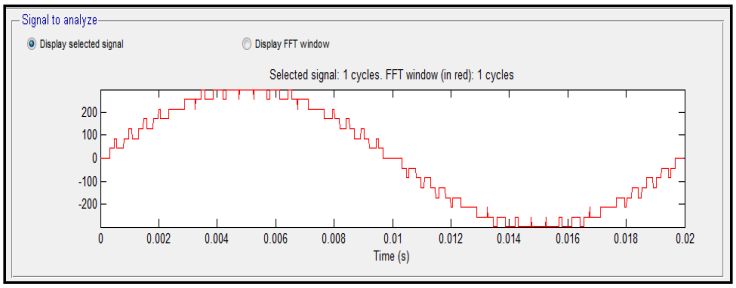

Figure 4.4: Signal of FFT Analysis for Optimal structure of the first proposed system

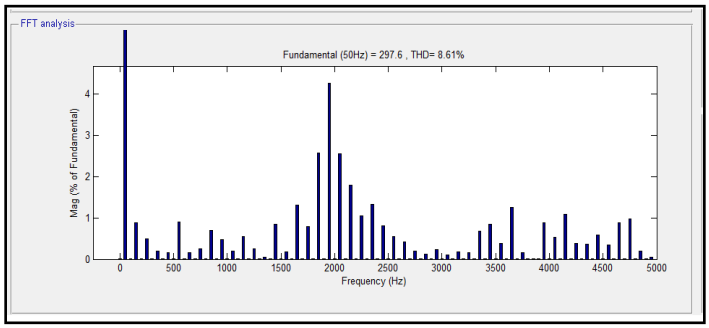

Figure 4.5 Bar chart of FFT Analysis for optimal structure

SIMULATION RESULTS FOR THE SECOND PROPOSED SYSTEM:

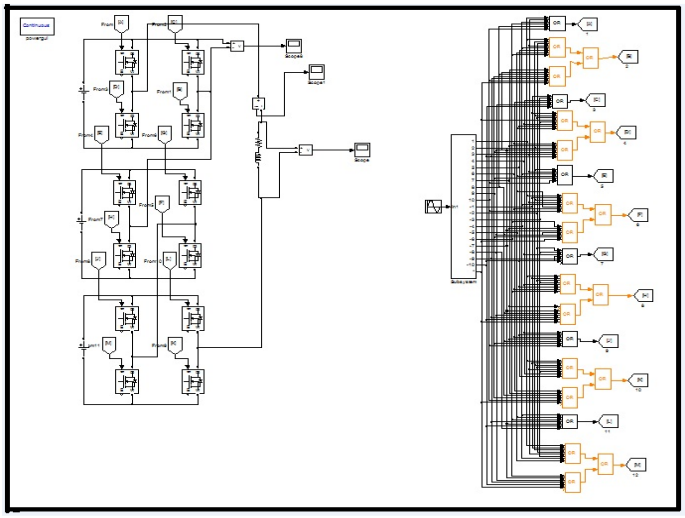

Figure 4.6 Simulink model of Optimal Structure (Second Algorithm) for Cascaded Multilevel DC link Inverter

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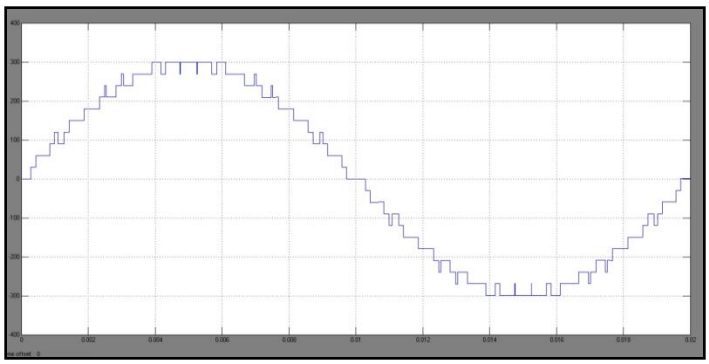

Figure 4.7 Output voltage Waveform for the Second proposed system

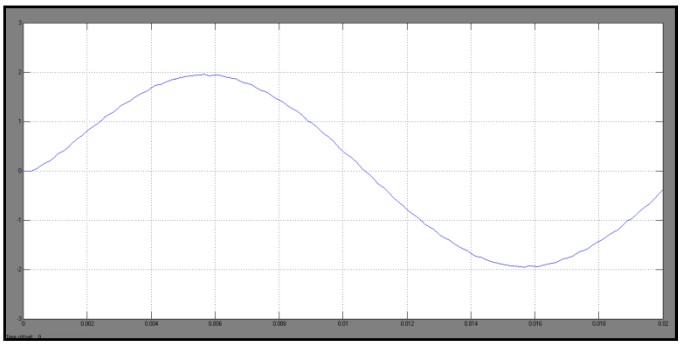

Figure 4.8 Output current Waveform for the Second proposed system

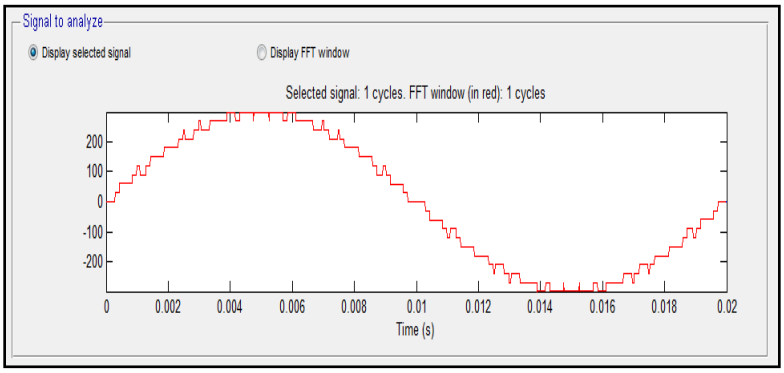

Figure 4.9 Signal of FFT Analysis for Optimal structure of the Second proposed system

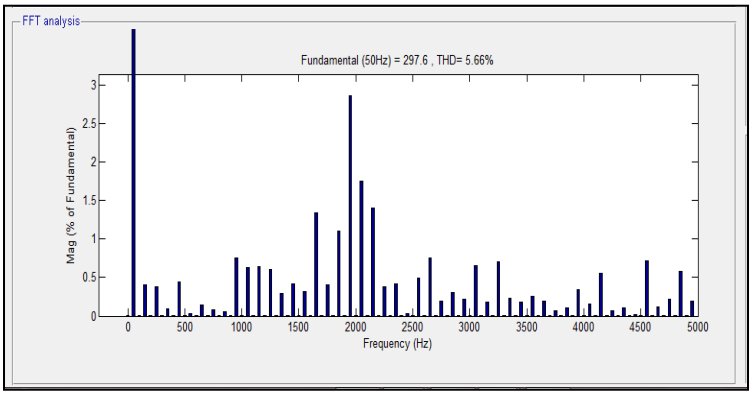

Figure 4.10 Bar chart of FFT Analysis for optimal structure

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TOPOLOGY – 2
SIMULATION RESULTS FOR THE FIRST PROPOSED SYSTEM:

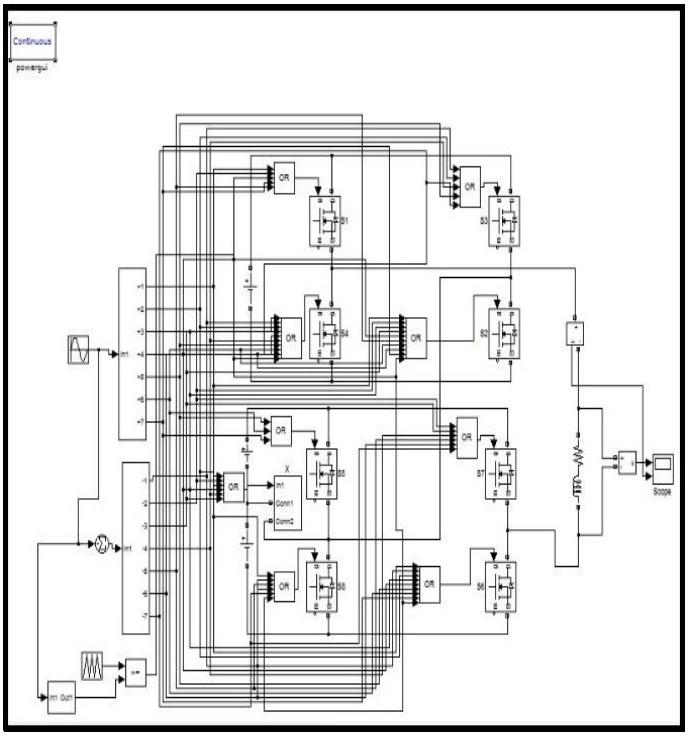

Figure 4.11Simulink model of Optimal Structure (First Algorithm) for 5 Level Transistor Clamped Multilevel DC link Inverter

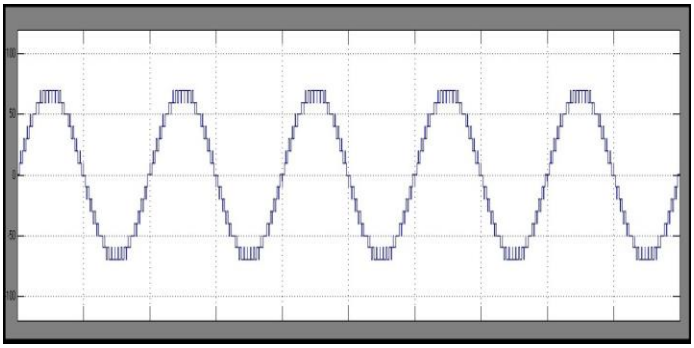

Figure 4.12 Output voltage Waveform for the First proposed system

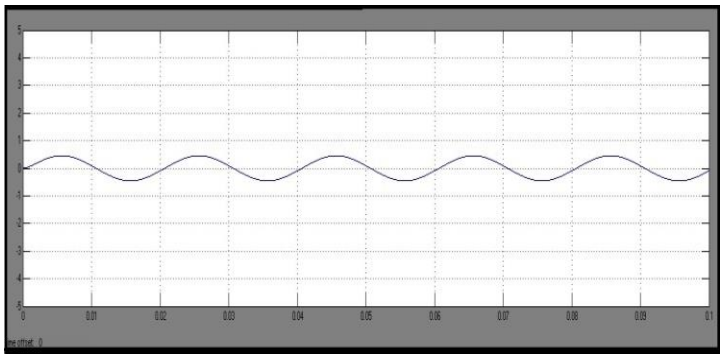

Figure 4.13 Output current Waveform for the First proposed system

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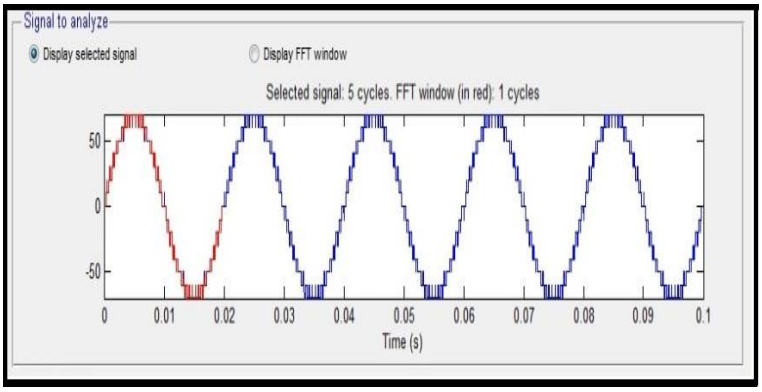

Figure 4.14 Signal of FFT Analysis for Optimal structure of the first proposed system

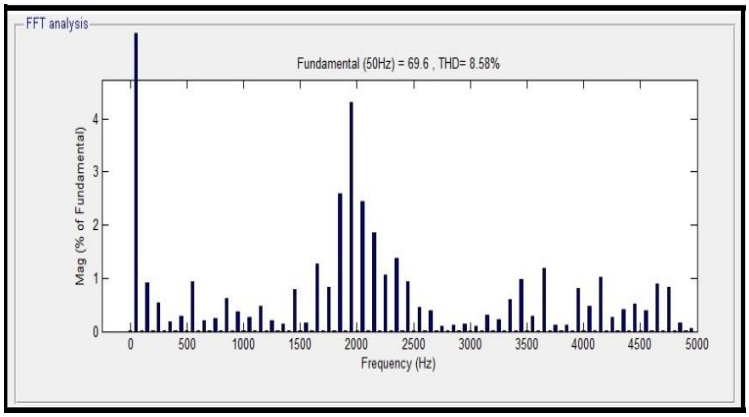

Figure 4.15 Bar chart of FFT Analysis for optimal structure

SIMULATION RESULTS FOR THE SECOND PROPOSED SYSTEM:

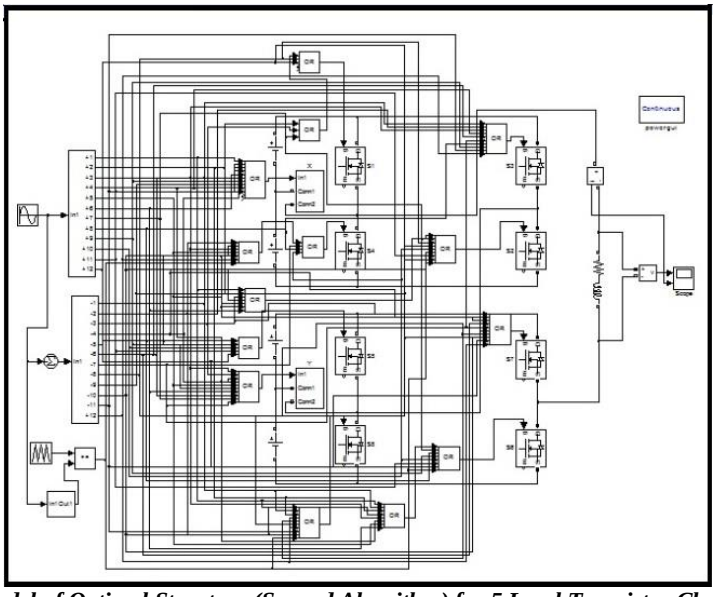

Figure 4.16 Simulink model of Optimal Structure (Second Algorithm) for 5 Level Transistor Clamped Multilevel DC link Inverter

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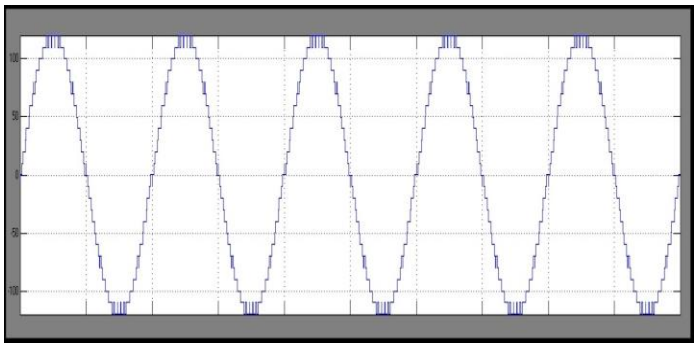

Figure 4.17 Output voltage Waveform for the Second proposed system

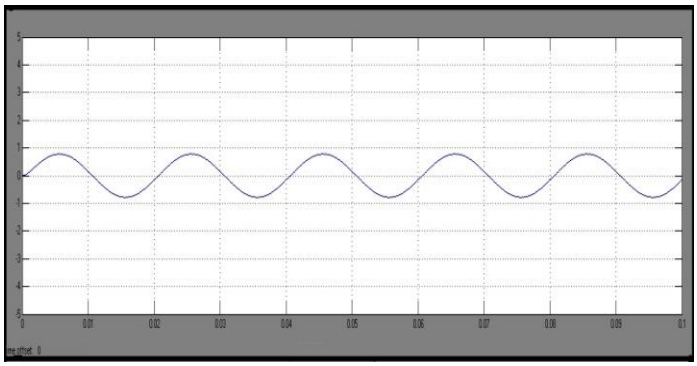

Figure 4.18 Output current Waveform for the Second proposed system

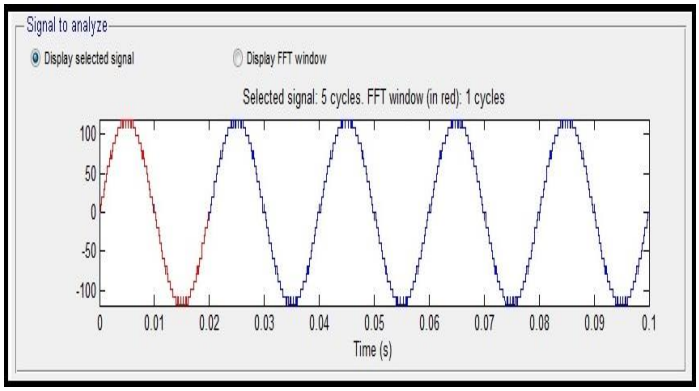

Figure 4.19 Signal of FFT Analysis for Optimal structure of the Second proposed system

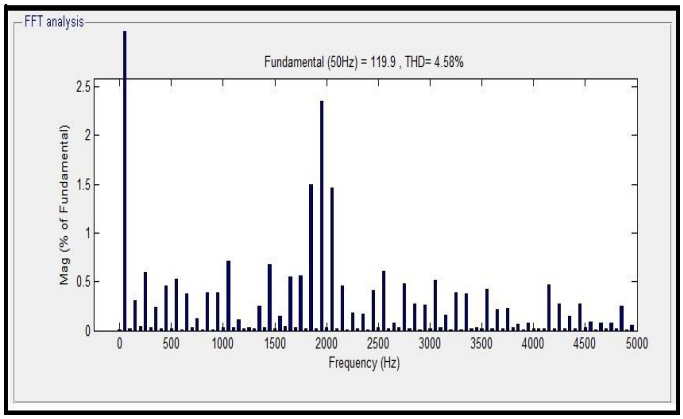

Figure 4.20 Bar chart of FFT Analysis for optimal structure

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V. CONCLUSION

Two new algorithms for the determination of the magnitudes of dc voltage sources have been proposed for two different Multilevel Inverter Topologies. These algorithms can provide all steps. It was shown that the structure consisting of units with two dc voltage sources is the best case to keep the minimum number of switches for a certain number of voltage steps. In addition, it was proven that these two topologies, consisting of units with one dc voltage source, is the optimal structure for minimizing the standing voltage on the switches, and that it minimizes the number of dc voltage sources.

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